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(71) Applicant: **NIPPON PRECISION CIRCUITS LTD.**
6-21, Kyobashi 2-chome,
Chuo-ku
Tokyo(JP)

(72) Inventor: **Miyabe, Saturo, c/o Nippon Precision Circuits Ltd**
3-9, Taihei 4-chome,
Sumida-ku
Tokyo(JP)
Inventor: **Toyama, Akira, c/o Nippon Precision Circuits Ltd**
3-9, Taihei 4-chome,
Sumida-ku
Tokyo(JP)
Inventor: **Takeda, Minoru, c/o Nippon Precision Circuits Ltd**
3-9, Taihei 4-chome,
Sumida-ku
Tokyo(JP)

(74) Representative: **Patentanwälte Grünecker, Kinkeldey, Stockmair & Partner**
Maximilianstrasse 58
D-80538 München (DE)

(54) Sampling rate converter.

(57) The invention is intended to provide an accurate sampling rate converter capable of operating stably.

[Configuration]

The converter comprises a sampling rate ratio-generating circuit 17 for creating data *d* about the ratio of the output sampling rate f_{so} to the input sampling rate f_{si}, a fine adjustment circuit 18 for finely adjusting the data *d*, using corrective data *p*, a forecasting circuit 19 for generating forecasted output timing data *g* about the timing at which output data Dou is delivered according to output data *e* from the fine adjustment circuit 18, a comparison-and-correcting circuit 21 for comparing the data *g* with data *m* and creating corrective data *p* from the results of the comparison, and an arithmetic circuit 12 on the output side. The data *m* indicates the timing at which the output data Dou is actually delivered. The arithmetic circuit 12 creates the output data Dou from both input data D*in* and data *g*.

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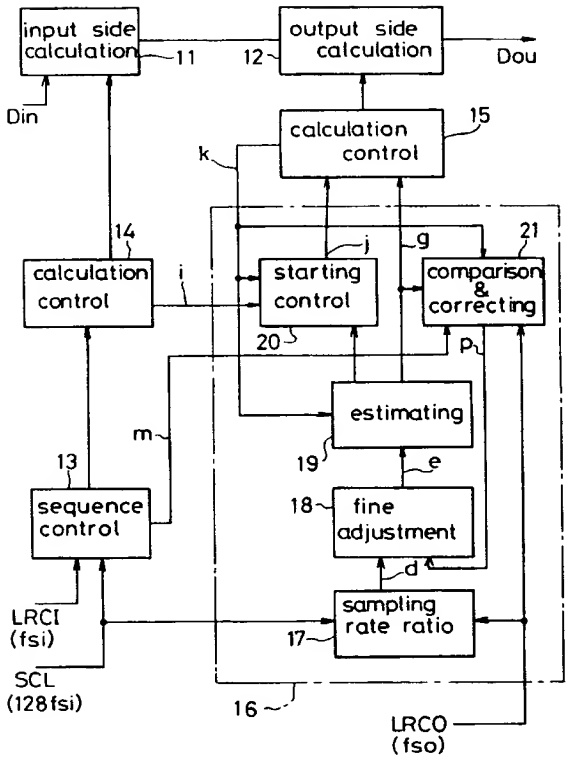
FIG.1



Detailed Description of the Invention

Industrial Field of Utilization

The present invention relates to a sampling rate converter used in digital audio applications and other similar applications.

Prior Art Techniques

Digital signals used in digital audio applications and other similar applications are sampled at rates which are different among different systems. Therefore, in order to exchange data among the different systems, it is necessary to convert one sampling rate into another. An apparatus which converts one sampling rate into another while maintaining the waveforms of audio signals or the like in this way is known as a sampling rate converter.

When the output sampling timing is asynchronous with the input sampling timing, or when the ratio of the output sampling rate to the input sampling rate cannot be expressed in terms of a simple combination of integers, the ratio of the output sampling rate to the input sampling rate is accurately found, and then the sampling rate is converted into a different value, based on the accurately found ratio. In the prior art techniques, both input sampling rate and output sampling rate have been averaged in order to accurately find the sampling rate ratio.

Problems to be Solved by the Invention

However, in order to secure high accuracy, it is necessary to make the averaging timing very long. Therefore, if the input and output sampling rates jitter at all, then the number of items of data calculated is not coincident with the number of items of data actually delivered. In this way, a malfunction takes places.

It is an object of the present invention to provide an accurate sampling rate converter capable of operating stably.

Means for Solving the Problems

The present invention lies in a sampling rate converter for converting a first signal of a first sampling rate into a second signal of a second sampling rate, said sampling rate converter comprising: a first data-generating circuit for generating first data about ratio of said second sampling rate to said first sampling rate; a second data-generating circuit for generating second data by correcting said first data, using a corrective data; a third data-generating circuit for generating, based on said second data, third data which corresponds to estimated output timing of said second signal;

a comparator circuit for generating comparative data by comparing said third data with fourth data which corresponds to actual output timing of said second signal; a correcting circuit for generating said corrective data, based on said comparative data; and

a second signal-generating circuit for generating said second signal based on said first and third data.

Embodiments

A first embodiment of sampling rate converter according to the present invention is hereinafter described by referring to Figs. 1, 2, 3, and 4. Fig. 1 is a block diagram showing the whole structure of the sampling rate converter. Fig. 2 is a block diagram, particularly showing the structure of a timing data-generating block 16 shown in Fig. 1. Fig. 3 is a timing chart illustrating the operation of the structures shown in Figs. 1 and 2. Fig. 4 is a diagram illustrating an interpolation operation performed by the sampling rate converter.

First, the structure of the first embodiment is described by referring to Figs. 1 and 2.

A calculation circuit 11 on the input side and an calculation circuit 12 on the output side mainly act to perform arithmetic operations for interpolation. These arithmetic operations for interpolation are described by referring to Fig. 4. The sampling rate converter of the described embodiment converts input data Din of sampling frequency f_{si} into output data Dou of sampling frequency f_{so}. During the conversion, arithmetic operations for interpolation (hereinafter referred to as the arithmetic operations on the input side) are performed about sampling points Pin corresponding to the input data Din by digital filtering techniques. In this manner, interpolated points C1, C2, and C3 are found. However, the interpolated points C1, C2, and C3 on the time axis t do not generally agree with the sampling points Pou corresponding to the output data Dou. Accordingly, arithmetic operations for an interpolation such as a linear interpolation (hereinafter referred to as the arithmetic operations on the output side) are carried out for adjacent interpolated points to find output data Dou corresponding to the sampling points Pou on the output side. The arithmetic circuit 11 on the input side mainly serves to perform the arithmetic operations on the input side. The arithmetic circuit 12 on the output side principally acts to perform the arithmetic operations on the output side.

A sequence control circuit 13 controls the whole operation of the sampling rate converter. This control circuit 13 receives input word clock

pulses LRCI having a frequency of f_{si} corresponding to the input sampling rate and system clock pulses SCL having a frequency of 128 f_{si} and produces a starting signal to a calculation control circuit 14. Also, the control circuit 13 produces data *m* on a reference time to a comparison-and-correcting circuit 17. The data *m* on the reference time indicates a reference time on which the whole system is based. Various kinds of timing data are created from this reference time data.

The calculation control circuit 14 controls the calculation circuit 11 on the input side. Another calculation control circuit 15 controls the arithmetic circuit 12 on the output side.

The individual components of the timing data-generating block 16 are now described. First, the main functions of the timing data-generating block 16 are described. The output data Dou are produced in synchronism with the output word clock pulses LRCO having a frequency of f_{so} corresponding to the output sampling rate. Therefore, arithmetic operations performed by the calculation circuit 12 on the output side for generating the output data Dou are preferably carried out, based on actual output timing data produced when the output word clock pulses LRCO are produced, i.e., based on the data *m* on the reference time when the output word clock pulses LRCO are produced. However, in order to create the output data Dou, some calculational time is needed. For this reason, it is impossible to perform the calculation, directly using the data *m* on the reference time. Accordingly, actual output timing is estimated (forecasted) and estimated (forecasted) output timing data *g* is created by the timing data-generating block 16. The calculation circuit 12 on the output side performs the calculation, based on the estimated (forecasted) output timing data *g*. It follows that a difference, or an error, is produced between the estimated (forecasted) output timing data *g* and the actual output timing data, i.e., the data *m* on the reference time. As described later, the timing data-generating block 16 makes this error infinitesimal.

The sampling rate ratio-generating circuit 17 creates data *d* about the ratio of the output sampling rate to the input sampling rate. Since the data *d* is used to generate the estimated (forecasted) output timing data *g* which is required to be quite accurate, the data *d* is generated with high accuracy. Counters 31, 32, a pulse generator circuit 33, and a latch 34 shown in Fig. 2 principally correspond to the sampling rate ratio-generating circuit 17.

A fine adjustment circuit 18 corrects the data *d*, using corrective data *p* described later, and generates more accurate data *e*. An adder 35 shown in Fig. 2 mainly corresponds to this fine adjustment circuit 18.

A estimating (forecasting) circuit 19 receives the data *e* and generates the estimated (forecasted) output timing data *g* under the control of an output side calculation end signal *k* from the calculation control circuit 15. The output side calculation end signal *k* is a signal indicating the end of each calculation performed by the arithmetic circuit 12 on the output side. An adder 36 and a latch 37 shown in Fig. 2 mainly correspond to this forecasting circuit 19.

A starting control circuit 20 creates an output side calculation starting request signal *j* under the control of both an input side calculation end signal *i* from the calculation control circuit 14 and the output side calculation end signal *k* from the calculation control circuit 15. The input side calculation end signal *i* is a signal indicating the end of each calculation performed by the calculation circuit 11 on the input side. The output side calculation starting request signal *j* is a signal requiring a start of calculation at the arithmetic circuit 12 on the output side.

A subtractive counter 38 and a gate 39 shown in Fig. 2 mainly correspond to this starting control circuit 20.

The comparison-and-correcting circuit 21 compares the estimated (forecasted) output timing data *g* with the actual output timing data, i.e., the data *m* on the reference time, and creates corrective data *p* from the results of the comparison (also referred to as the corrective data herein). The timing of the comparison operation is synchronized to the output word clock pulses LRCO. An FIFO buffer 40, an adder 41, a 1/N circuit 42, and a latch 43 shown in Fig. 2 mainly correspond to this comparison-and-correcting circuit 21.

The operation of the embodiment shown in Figs. 1 and 2 is described next by referring to the timing chart of Fig. 3.

The counter 31 forwardly counts the output word clock pulses LRCO of the frequency f_{so}, and produces output *a* whenever 2048 pulses are counted. The counter 32 forwardly counts the system clock pulses SCL having the frequency of 128 f_{si}. The pulse generator circuit 33 receives the output *a* from the counter 31 and produces a latch pulse *b* on every leading edge of the system clock pulses SCL. On the leading edge of this latch pulse *b*, the count value *c* of the counter 32 is latched in the latch 34. On the trailing edge, the count value of the counter 32 is set to 1. As a result, the output data *d* from the latch 34 is $2048 \times 128 \times (f_{si}/f_{so})$. In consequence, accurate data about the ratio of the output sampling rate to the input sampling rate is derived.

The adder 35 produces the sum of the data *d* from the latch 34 and the corrective data *p* from the latch 43. Although the data *d* itself is suffi-

ciently accurate data, a fine adjustment is made, using the corrective data *p*. In this way, more accurate data *e* is obtained.

The adder 36 calculates the sum of the data *e* and the estimated (forecasted) output timing data *g* from the latch 37 and produces 22-bit data *f*. The lower significant 19 bits of the data *f* are latched in the latch 37 in response to the output side calculation end signal *k*. The upper 3 bits are preset into the subtractive counter 38, which is decremented by every application of the input side calculation end signal *i*. When the output *h* from the subtractive counter 38 decreases down to 0, the gate 39 produces the output side calculation starting request signal *j*, so that the calculation circuit 12 on the output side starts a sequence of calculations on the output side. When this sequence ends, the output side calculation end signal *k* becomes active. In this way, whenever the signal *k* becomes active, the estimated (forecasted) output timing data *g* from the latch 37 is replaced by successive new data.

The estimated (forecasted) output timing data *g* is successively accepted into the FIFO buffer 40 in response to the output side calculation end signal *k* and successively delivered from the buffer 40 in response to the output word clock pulses LRCO. Output data "1" from the FIFO buffer 40 is applied to the negative input terminal of the adder 41, while the data *m* on the reference time is applied to the positive input terminal of the adder 41. That is, the estimated (forecasted) output timing data *g* is compared with the data *m* on the reference time (corresponding to the actual output timing) at the timing of the output word clock pulses LRCO. Data about the resulting error (referred to as the error data herein) is produced from the adder 41. The error data *n* from the adder 41 is reduced by a factor of 2048 by the 1/N circuit 42. The reduced data *o* is latched in the latch 43 in response to the output word clock pulses LRCO. The output from the latch 43 is applied as the corrective data *p* to the adder 35. The error data *n* is diminished by the 1/N circuit 42, because if the corrective data *p* is too large, then the effect of every instantaneous variation becomes great, thus risking the stability.

In the present embodiment, the data *d* itself about the ratio of the output sampling rate to the input sampling rate is sufficiently accurate. However, if the embodiment relies only on this, and if the input and output sampling rates jitter at all, then the error between the estimated (forecasted) output timing and the actual output timing might be accumulated. Therefore, the data *d* is finely adjusted, using the corrective data *p*. Thus, accurate and stable, estimated (forecasted) output timing data *g* is generated.

A second embodiment of sampling rate converter according to the present invention is described next by referring to Fig. 5.

As can be seen from Figs. 2 and 5, the second embodiment is similar to the first embodiment except that a nonlinear correcting circuit 42a is provided instead of the 1/N circuit 42 (linear correcting circuit) of the first embodiment.

In the first embodiment shown in Fig. 2, to prevent malfunction due to variations in the input and output sampling rates, corrections are made by using the 1/N circuit 42 (linear correcting circuit) in a correcting circuit. In order to carry out the corrections, the corrections must be highly accurate for minute variations in the input and output sampling rates. The corrections must show good response to great variations in the input and output sampling rates. However, in the 1/N circuit 42 of the first embodiment, if the value of N is increased, the correction accuracy is improved but the response to variations in the sampling rates deteriorates. Conversely, if the value of N is reduced, the response to variations in the sampling rates is improved but the correction accuracy is deteriorated. To satisfy these two requirements, it is necessary to switch the value of N according to the amounts of change in the input and output sampling rates or to increase the number of stages of the FIFO buffer 40.

Accordingly, in the second embodiment, accurate corrections are made in response to minute variations in the input and output sampling rates. Corrections are made with good response to great variations in the input and output sampling rates. For this purpose, the nonlinear correcting circuit 42a shown in Fig. 5 is provided as a correcting circuit. This correcting circuit 42a creates an odd power (e.g., the third power) of the input data *n* as output data *o*. The relation of the output to the input, which corresponds to the relation of the error data *n* to the corrective data *p*, is shown in Fig. 6. In this nonlinear correcting circuit 42a, minute error data *n* close to the origin of the graph of Fig. 6 are further reduced to create the corrective data *p*. This is because if the corrective data *p* is too great compared with the error data *n*, the effect of every instantaneous error variation becomes great. This might deteriorate the stability. In the nonlinear correcting circuit 42a, great error data *n* remote from the origin of the graph of Fig. 6 are amplified, thus creating corrective data *p*. This is intended to make corrections with good response to great variations in the input and output sampling rates. In the nonlinear correcting circuit 42a, the corrective data *p* is created, for example, according to a cubic curve. Therefore, just when the error begins to increase, the amplification factor does not increase rapidly. Rather, the circuit can smoothly follow the

error.

Generally, input data *n* supplied to the nonlinear correcting circuit 42a and output data *o* from it take digital form. Therefore, the relation of the output to the input to the nonlinear correcting circuit 42a can be expressed by bent lines as shown in Figs. 7 and 8. Generally speaking, this nonlinear correcting circuit 42a acts to generate output data *o* (corresponding to the corrective data *p*) in such a way that the rate of increase of the absolute value of the output data *o* (corresponding to the corrective data *p*) with respect to increase in the absolute value of the input data *n* (the error data *n*) increases as the absolute value of the input data *n* - (the error data *n*) increases. Alternatively, the relation of the output data *o* (corresponding to the corrective data *p*) to the input data *n*, or the error data *n*, is based on such a function that the rate of increase of the absolute value of the output data *o* (corresponding to the corrective data *p*) with respect to increase in the absolute value of the input data *n* (the error data *n*) increases as the absolute value of the input data *n* (the error data *n*) increases, and the nonlinear correcting circuit digitally approximates the function and creates corrective data.

In the present second embodiment, the data *d* about the ratio of the output sampling rate to the input sampling rate is sufficiently accurate, in the same way as in the first embodiment. However, if the embodiment relies only on this, and if the input and output sampling rates jitter at all, then the difference, or an error, between the estimated (forecasted) output timing and the actual output timing might be accumulated. When either the input or output sampling clock is varied to thereby induce great variations, there arises a possibility that a very great difference is produced between the estimated (forecasted) output timing and the actual output timing. Thus, the data *d* is adjusted, using the corrective data *p*. The estimated (forecasted)output timing data *g* showing accurate and stable characteristics for small variations in the input and output sampling rates and exhibiting quick and smooth response to great variations in the input and output sampling rates is created.

Effects of the Invention

The present invention permits fabrication of an accurate sampling rate converter capable of operating stably.

Brief Description of the Drawings

Fig. 1 is a block diagram showing the whole structure of a sampling rate converter according to the present invention;

Fig. 2 is a block diagram of a first embodiment of the invention, particularly showing a timing data-generating block 16 shown in Fig. 1;

Fig. 3 is a timing chart illustrating the operation of the converter shown in Figs. 1 and 2;

Fig. 4 is a diagram illustrating an interpolation operation performed by the sampling rate converter shown in Fig. 1;

Fig. 5 is a block diagram of a second embodiment of the invention, particularly showing the timing data-generating block 16 shown in Fig. 1;

Fig. 6 is a graph showing an input-output characteristic of a nonlinear correcting circuit shown in Fig. 5;

Fig. 7 is a graph showing another input-output characteristic of the nonlinear correcting circuit shown in Fig. 5; and

Fig. 8 is a graph showing a further input-output characteristic of the nonlinear correcting circuit shown in Fig. 5.

Legends:

12:	calculation circuit on the output side (second signal-generating circuit)
17:	sampling rate ratio-generating circuit (first data-generating circuit)
18:	fine adjustment circuit (second data-generating circuit)
19:	estimating circuit (third data-generating circuit)
21:	comparison-and-correcting circuit
Din:	first signal
Dou:	second signal
d:	first data
e:	second data
g:	third data
m:	fourth data
n:	error data
p:	corrective data

Claims

1. A sampling rate converter for converting a first signal of a first sampling rate into a second signal of a second sampling rate, said sampling rate converter comprising:

a first data-generating circuit for generating first data which corresponds to ratio of said second sampling rate to said first sampling rate;

a second data-generating circuit for generating second data by correcting said first data, using a corrective data;

a third data-generating circuit for generating, based on said second data, third data which corresponds to estimated output timing of said second signal;

a comparator circuit for generating comparative data by comparing said third data with fourth data which correponds to actual output timing of said second signal;

a correcting circuit for generating said corrective data, based on said comparative data; and

a second signal-generating circuit for generating said second signal based on said first and third data.

2. The sampling rate converter of claim 1, wherein said comparative data is error data indicative of a difference between said third data and said fourth data.

3. The sampling rate converter of claim 2, wherein said correcting circuit generates said corrective data by multiplying said error data by a factor of (1/constant value).

4. The sampling rate converter of claim 2, wherein said correcting circuit generates said corrective data in such a way that rate of increase of absolute value of said corrective data with respect to increase in absolute value of said error data increases as absolute value of said error data increases.

5. The sampling rate converter of claim 2, wherein a relation between said error data and said corrective data is based on such a function that rate of increase of absolute value of said corrective data with respect to increase in absolute value of said error data increases as absolute value of said error data increases, and wherein said correcting circuit digitally approximates said function and generates said corrective data.

FIG. 1

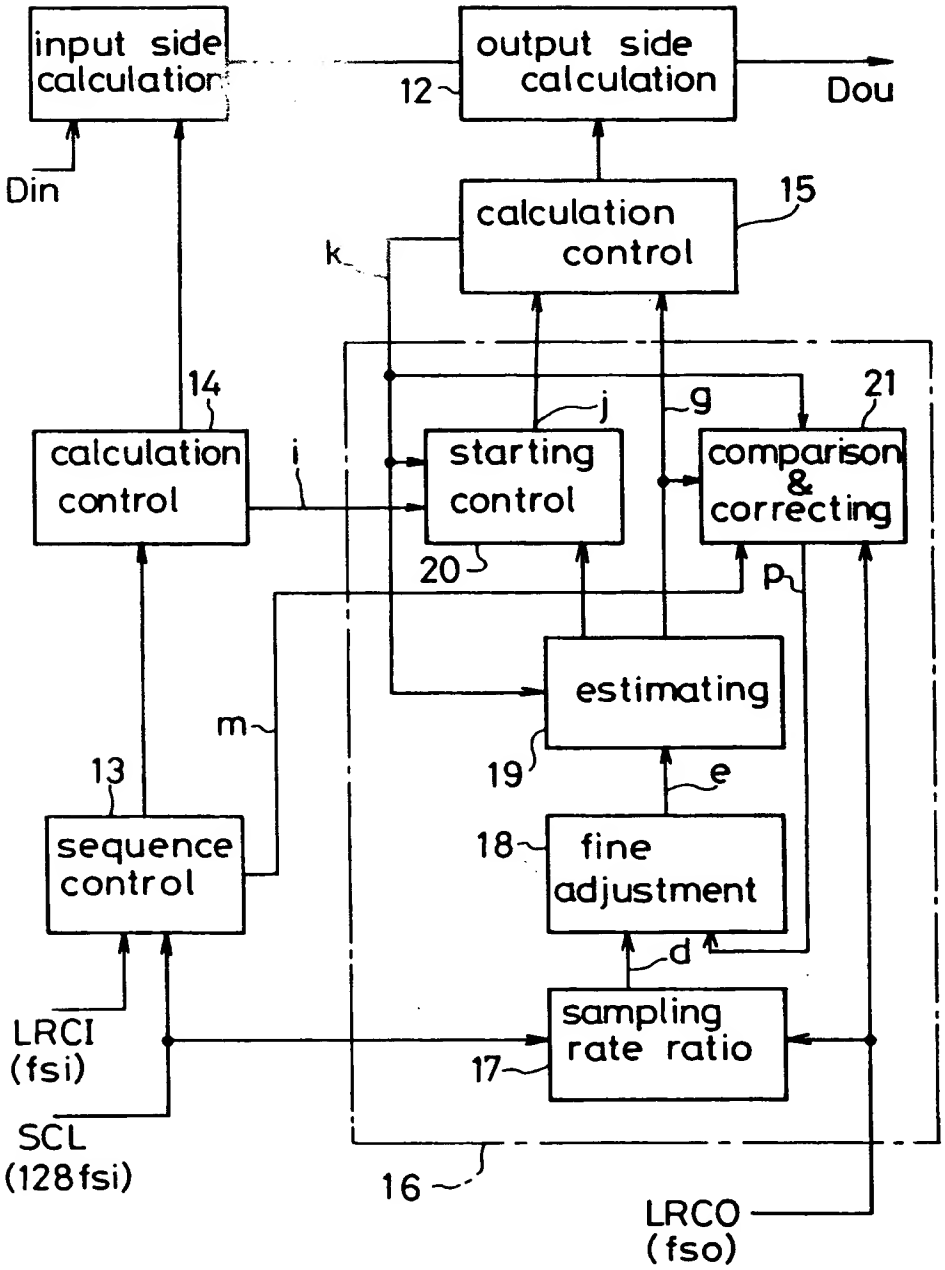


FIG. 2

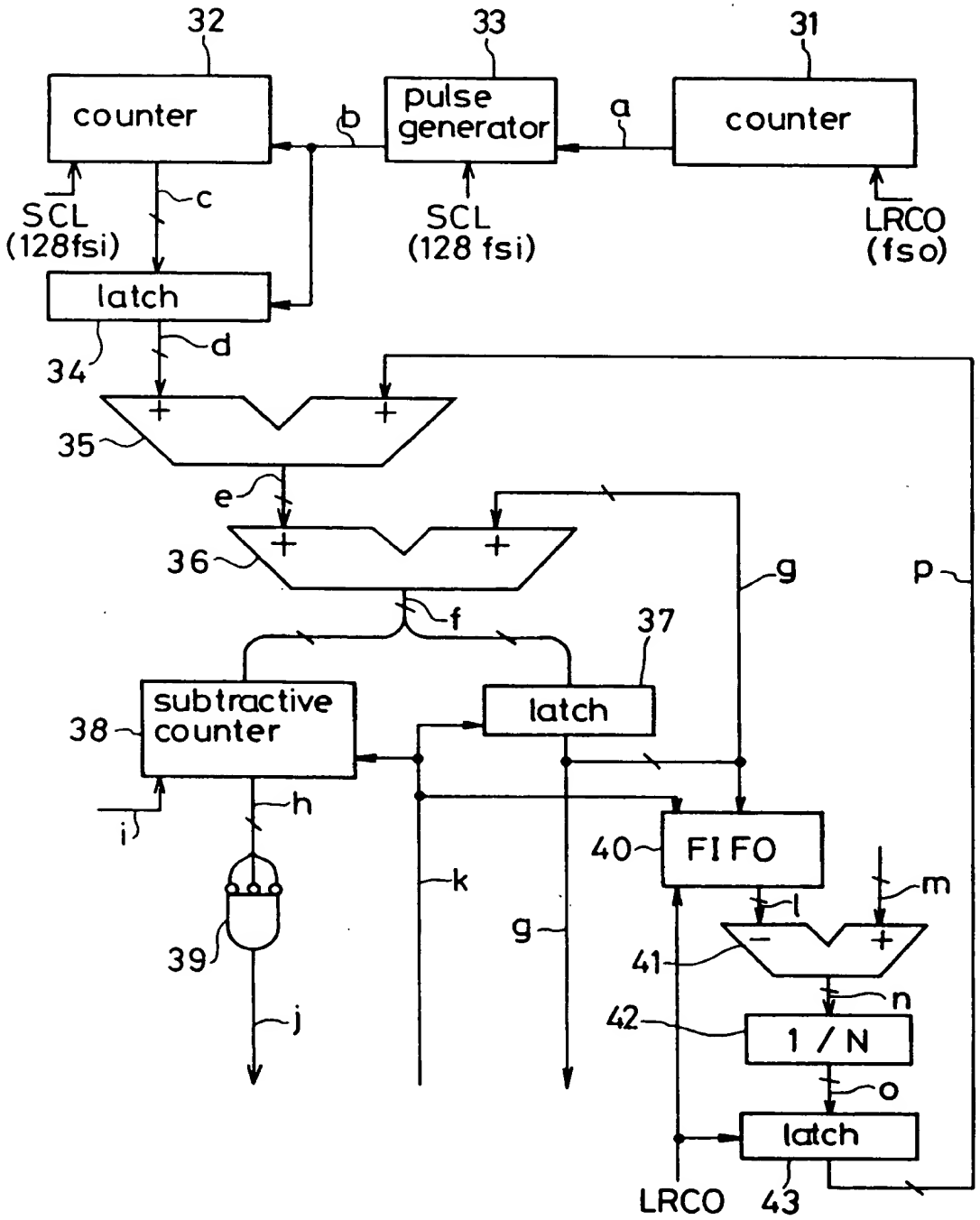

32
33
31
counter
pulse generator
counter
b
a
c
SCL (128fsi)
SCL (128 fsi)
LRCO (fso)
latch
d
34
35
e
36
g
p
f
37
subtractive counter
38
latch
h
i
40
FIFO
m
l
k
g
41
39
n
42
1 / N
j
o
latch
LRCO
43

FIG. 3

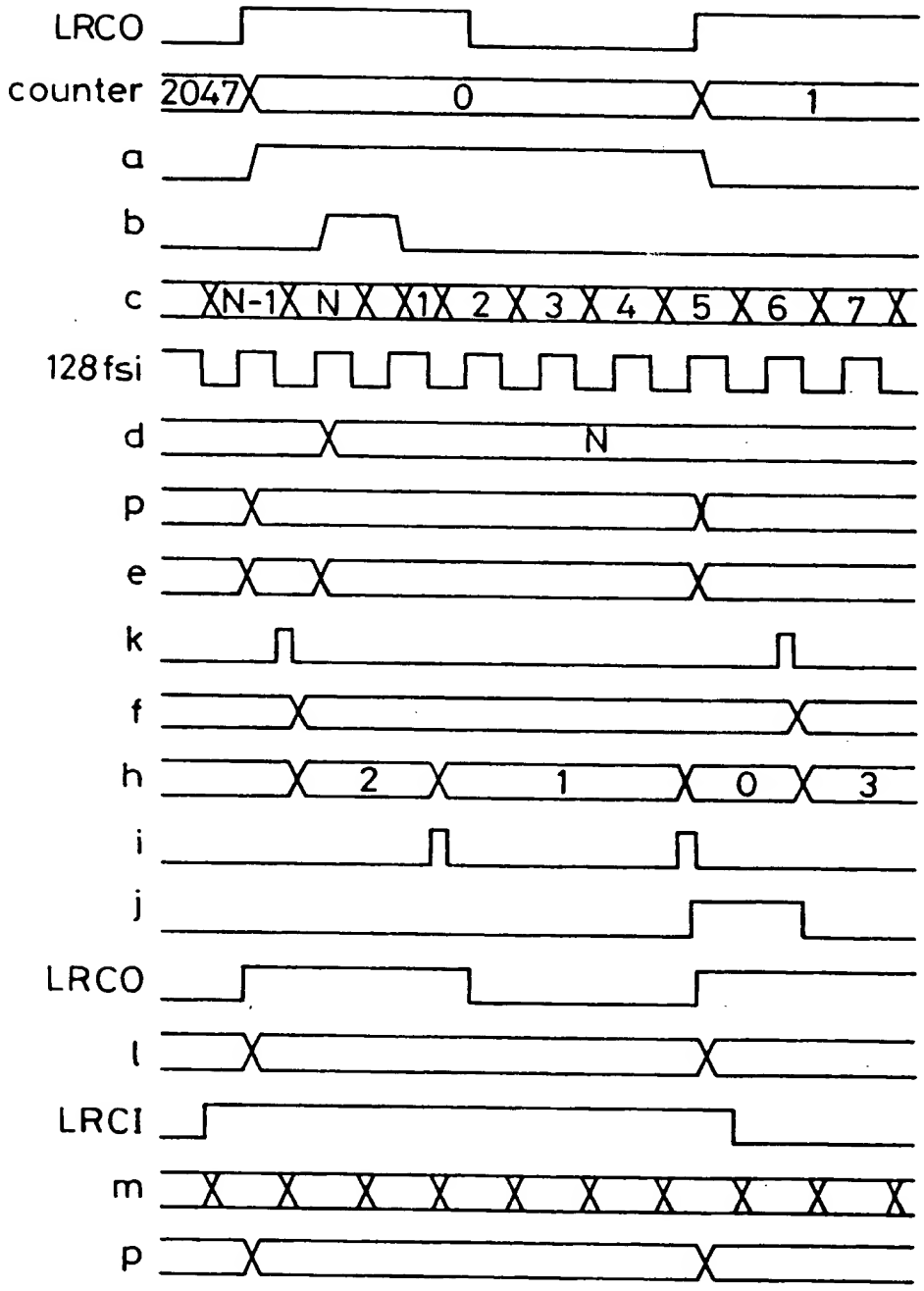

LRCO
counter
2047
0
1
a
b
c
N-1
N
1
2
3
4
5
6
7
128fsi
d
N
p
e
k
f
h
2
1
0
3
i
j
LRCO
l
LRCI
m
p

FIG.4

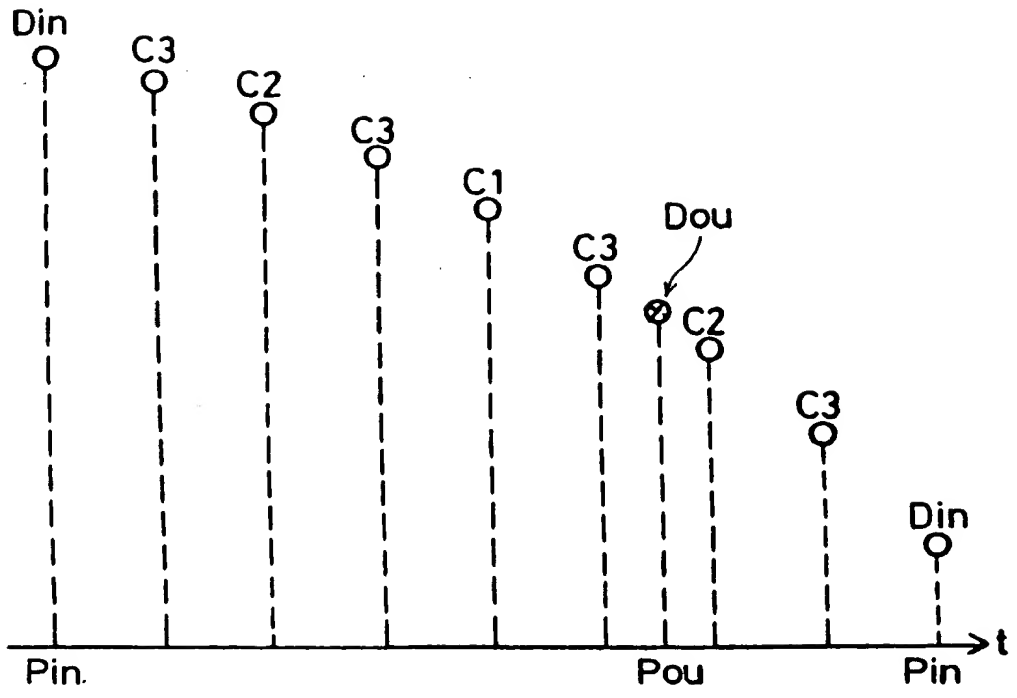


FIG. 5

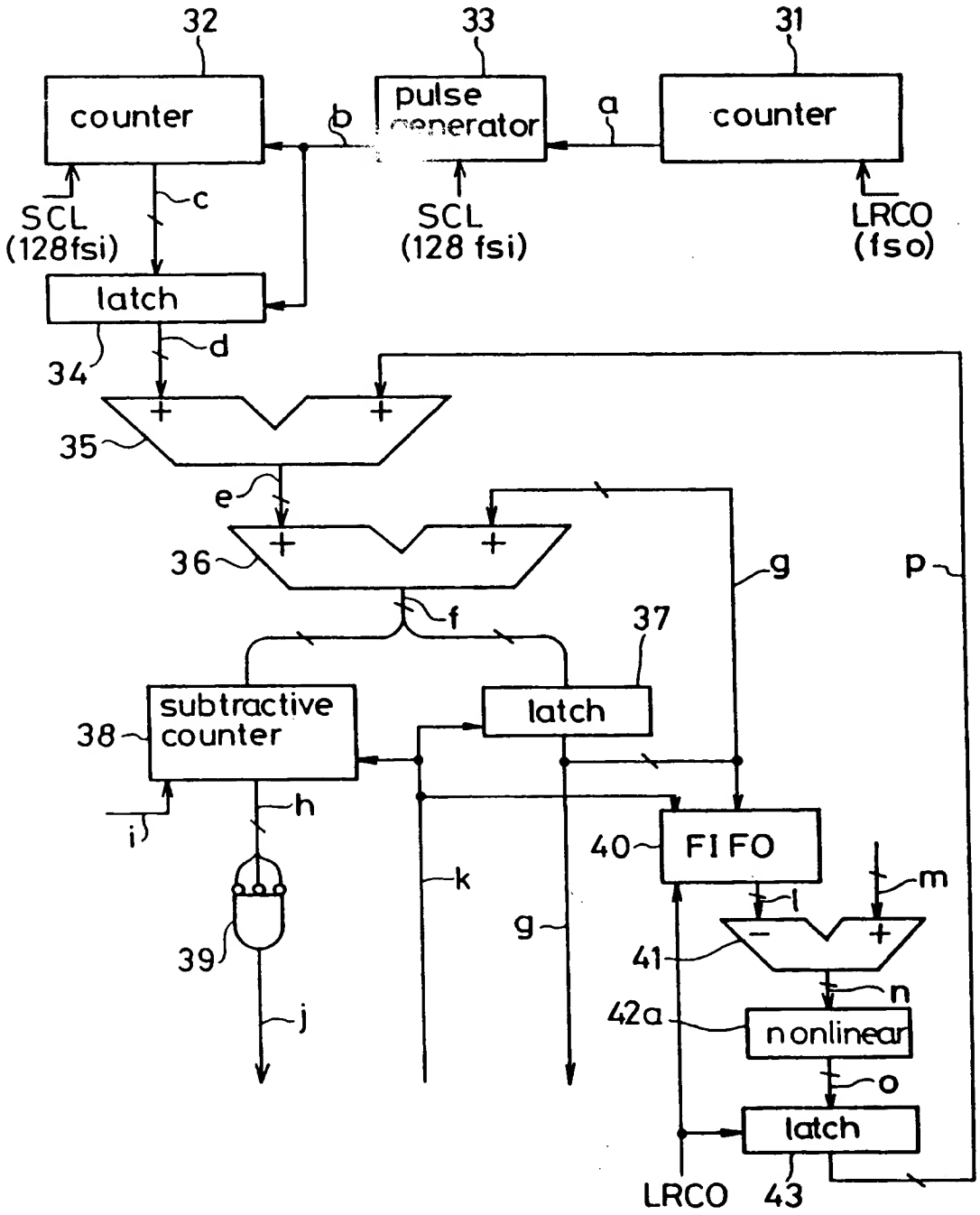


FIG.6

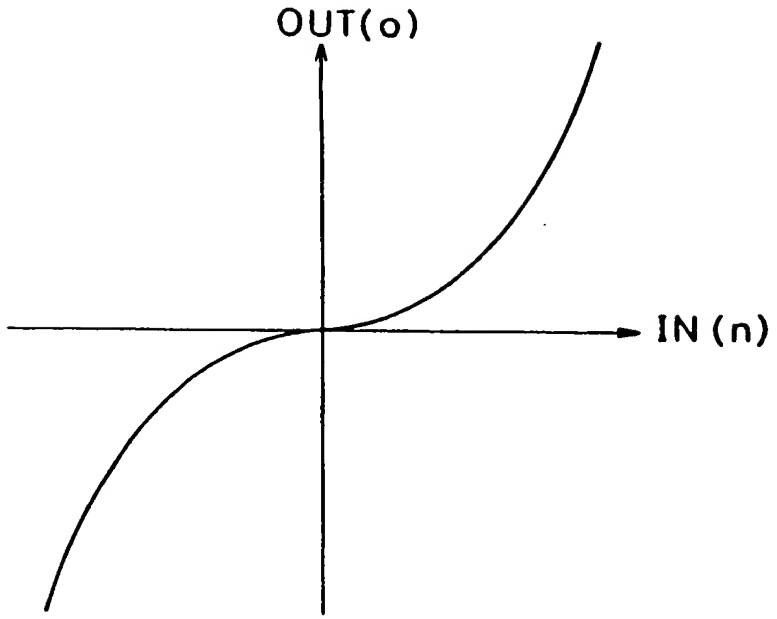


FIG.7

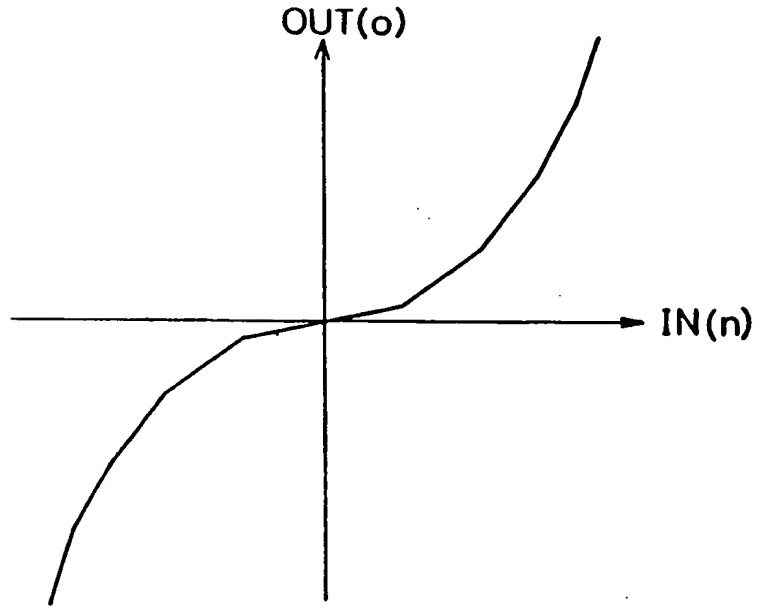
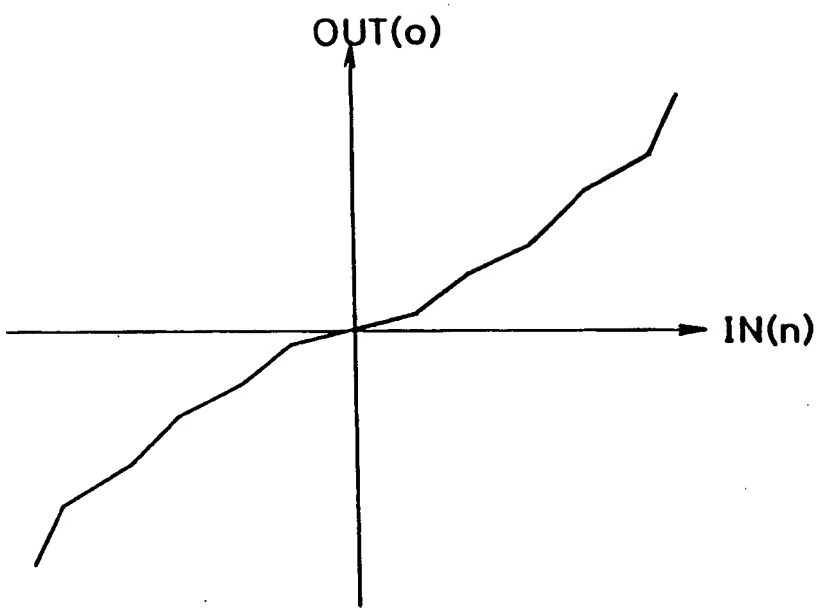


FIG. 8



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EUROPEAN SEARCH REPORT

Application Number
EP 93 12 1081

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	WO-A-92 17951 (FROX) 15 October 1992 * the whole document *	1	H03H17/06
A	US-A-4 896 334 (BABAK SAYAR) 23 January 1990 * the whole document *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H03H

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 April 1994	Coppieters, C

CATEGORY OF CITED DOCUMENTS

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